Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1367	(asic or fpga or (integrate$1 adj1 circuit)) same (mac or (media adj1 access))	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/09/22 10:38
L4	986	1 and (media adj1 access adj1 control$4)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/09/22 10:39
L6	294	(asic or fpga or (integrate$1 adj1 circuit)) same (mac or (media adj1 access)) same logic	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/09/22 11:26
L7	218	6 and (media adj1 access adj1 control$4)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/09/22 10:39
L8	123	(asic or fpga or (integrate$1 adj1 circuit)) same (mac or (media adj1 access)) same multi$1plex$3	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/09/22 11:26
S1	3149	asic and mac	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/09/22 10:13
S2	3477	((specific adj1 integrated adj1 circuit) or asic) and ((media adj1 access adj1 controller) or mac)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/03/31 15:18
S4	30	S2 and 370/400.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/03/31 15:52
S5	660	((specific adj1 integrated adj1 circuit) or asic) and ((media adj1 access adj1 controller) or mac) same logic	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 10:01
S6	141	S2 and 370/401.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/03/31 16:41
S7	28	S2 and 370/419.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/03/31 17:08
S8	11	S2 and 370/420.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/03/31 17:08

S9	18	S2 and 716/12-17.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/03/31 17:30
S10	11	S2 and 709/208.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/03/31 17:30
S11	1	S2 and 326/37.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 09:39
S12	3477	((specific adj1 integrated adj1 circuit) or asic) and ((media adj1 access adj1 controller) or mac)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 09:40
S13	28	S12 and 712/32,36,37.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 09:40
S15	26	S12 and 713/2,100.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 10:01
S16	2068	((specific adj1 integrated adj1 circuit) or asic or chip) same ((media adj1 access adj1 controller) or mac)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 13:03
S17	37	S16 and meta$1data	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 10:24
S18	273	S16 and ((arithmetic near3 unit) or alu)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 10:42
S20	1468	mac and ((arithmetic near3 unit) or alu)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 10:53
S22	119	S20 and (media adj1 access adj1 controller)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 12:57
S23	562	asic same mac	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 13:55

S24	176	S23 and (media adj1 access adj1 controller)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 13:55
S25	246	fpga same mac	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 13:55
S26	51	S25 and (media adj1 access adj1 controller)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/04/01 13:55